Claims:

1. A semiconductor chip package, comprising:

a. a semiconductor chip with bond pads thereon;

b. conductive leads electrically connected to the bond pads;

c. encapsulating material covering at least a portion of the chip and at least a portion of the conductive leads, the encapsulating material having openings therein to expose electrode bond areas on the conductive leads; and

d. electrodes contacting the electrode bond areas through the openings in the encapsulating material.

2. A semiconductor chip package according to Claim 1, wherein the bond pads are electrically connected to active devices formed in the chip.

3. A semiconductor chip package according to Claim 1, wherein the encapsulating material encapsulates the chip and the conductive leads extend out through the encapsulating material.

4. A semiconductor chip package according to Claim 1, wherein the encapsulating material encapsulates the chip and the conductive leads.

5. A semiconductor chip package according to Claim 1, wherein the electrodes comprise a plurality of solder balls each approximating the size and shape of the openings in the encapsulating material, the solder balls being bonded to the leads through the openings in the encapsulating material.

6. A semiconductor chip package, comprising:

a. a semiconductor chip having bond pads thereon, the bond pads being accessible from an upper surface of the chip;

b. conductive leads extending over and attached to the upper surface of the chip;

c. connecting means for electrically connecting the conductive leads to the bond pads;

d. encapsulating material covering at least a portion of the upper surface of the chip, the bond pads, at least a portion of the conductive leads and the connecting means, the encapsulating material having openings therein to expose electrode bond areas on the conductive leads; and

e. electrodes contacting the electrode bond areas through the openings in the encapsulating material.

7. A semiconductor chip package according to Claim 6, wherein the bond pads are electrically connected to active devices formed in the chip.

8. A semiconductor chip package according to Claim 6, wherein the bond pads are aligned along a central portion of the chip.

9. A semiconductor chip package according to Claim 6, wherein the conductive leads are attached to the upper surface of the chip by a layer of adhesive material interposed between the conductive leads and the upper surface of the chip.

10. A semiconductor chip package according to Claim 6, wherein the connecting means comprises a plurality of bond wires bonded to the conductive leads and the bond pads thereby electrically connecting the conductive leads to the bond pads.

11. A semiconductor chip package according to Claim 6, wherein the encapsulating material is a thermosetting epoxy resin.

12. A semiconductor chip package according to Claim 6, wherein the encapsulating material encapsulates the chip and the conductive leads extend out through the encapsulating material.

13. A semiconductor chip package according to Claim 6, wherein the encapsulating material encapsulates the chip, the bond pads, the connection means and the conductive leads.

14. A semiconductor chip package, comprising:

a. a semiconductor chip assembly comprising a semiconductor chip having bond pads thereon and discrete conductive leads at spaced apart locations superjacent to and in electrical contact with the bond pads, the semiconductor chip assembly being disposed within an encapsulating material; and

b. electrode bumps extending through the encapsulating material to contact the conductive leads and protruding from the encapsulating material for connection to an external circuit.

15. A semiconductor chip package according to Claim 14, wherein the conductive leads have an outer end that extends out from the encapsulating material.

16. A semiconductor chip package, comprising:

a. a semiconductor chip having active devices therein;

b. a plurality of bond pads electrically connected to the active devices, the bond pads being aligned along a central portion of one surface of the chip;

c. an insulating layer overlying the surface of the chip, the insulating layer having holes therein to enable electrical connection to the bond pads through the holes;

d. a plurality of discrete conducting leads extending over and attached to the insulating layer, each lead having an inner end and an outer end, the inner end being located in close proximity to the bond pads;

e. a plurality of bond wires bonded to wiring bond areas on the inner end of the leads and the bond pads on the chip thereby electrically connecting the leads to the bond pads;

f. an encapsulating material disposed over and enclosing the chip, the bond pads, the inner end of the conducting leads and the bond wires, the encapsulating material having openings formed therein to expose electrode bond areas on the inner end of the conductive leads; and

g. a plurality of solder balls each approximating the size and shape of the openings in the encapsulating material, the solder balls being bonded to the electrode bond areas through the openings in the encapsulating material.

17. A semiconductor chip package according to Claim 16, wherein the size and shape of the openings is defined by a desired size and shape of the solder balls after a reflow step.

18. A semiconductor chip package according to Claim 16, wherein the conductive leads are severed substantially flush with the encapsulating material after encapsulation.